

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT : Masao Watari et al.
SERIAL NO. : 10/542,103
FILING DATE : July 12, 2005
FOR : Operation Device, Operation Device
Designing Method, and Logic Circuit
Designing Method
EXAMINER : Joseph D. Torres
GROUP ART UNIT : 2112
CONFIRMATION NO. : 1068

6 Pages
Via EFS-Web
Mail Stop Election
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ELECTION WITH AMENDMENT

Sir:

In response to the Restriction Requirement dated February 17, 2009,
please amend the above identified application as follows: